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APPLICATION FOR LETTERS PATENT

TITLE: AUDIO SIGNAL PROCESSORS

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BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to audio signal processors.

Description of the Prior Art

Conventionally the audio band is deemed to be about DC to about 20KHz and frequencies above that range are ignored as inaudible. In fact the audio band rolls off, rather than abruptly ending at 20 KHz, and some people with expert listening skills consider that frequencies above 20KHz are audible or at least consider that they can hear the effects in the audible frequency band of frequency components outside that conventional band. In other words, frequencies above 20kHz may affect elements of the audio response in the conventional audio band.

SUMMARY OF THE INVENTION

According to the present invention, there is provided an audio signal processor which modifies audio signal components not only in the conventional audio band but also in the range of frequencies from the conventional upper limit of the conventional audio band to frequencies greater than 24kHz.

The conventional audio band is the range of frequencies from DC to 20kHz or from about 20Hz to 20kHz. Whilst DC is inaudible, some audio signal processors have a frequency response down to DC.

The said range of frequencies above 20kHz may extend to an upper limit of 30khz or to 50kHz or to 100kHz. The processor of the invention is able to modify components in the whole of the band from DC or 20Hz to the upper limit e.g. 100kHz. The modification may be equalization such as gain control, frequency dependent gain control, frequency/ phase characteristic control or any other form of modification conventional in the art.

It may be observed that some prior audio processors include transmission channels of bandwidth extending beyond 20kHz but that prior audio processors do not modify audio signals outside the conventional audio band as far as is known to the present inventor.

In an embodiment of the present invention, the said audio components are sampled and digitized to produce digital audio components.

In a preferred embodiment of the invention, the audio signal components are

sampled and digitized as 1-bit signals at a sampling rate of: e.g.198kHz or greater; or 1.4MHz or greater; or preferably about 2.85MHz e.g. 2.8224MHz (64x44.1kHz).

In the preferred embodiment, the processor includes a 1-bit Delta Sigma Modulator (DSM). The DSM may be a filter and/or a gain control and/or a signal adder or mixer. An example of a DSM is described hereinbelow.

The invention provides audio signal processing of very high quality. Although it appears unnecessary, according to conventional practice, to equalise over such wide frequency bands and at such high sampling rates as are used in the embodiments of the invention it is believed that so doing contributes to the fidelity of the processed audio signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the invention will be apparent from the following detailed description of illustrative embodiments which is to be read in connection with the accompanying drawings, in which:

Figure 1 is a block diagram of an audio signal processor according to the present invention;

Figure 2 is a schematic block diagram of an illustrative 1-bit audio signal mixer useful in the processor of Figure 1; and

Figure 3 is a schematic block diagram of an integrator of the mixer of Figure 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, an audio signal processor has an input 2 for receiving audio signals from for example a stereo pair of microphones 4. An anti-aliasing low-pass filter 6 passes signal components in the range of about DC to about 100kHz. The audio signals are sampled and digitized in an analogue to digital converter ADC 8.

The converter may be an n-bit converter where n is greater than one, e.g. 16 as is conventional in digital audio. The ADC 8 samples the signal at a suitable sample rate for n-bit digitization. The sample rate is set by a clock 12.

Preferably the converter 8 is a 1-bit converter. It may have a sampling rate of 198kHz or greater than 1.4Mhz preferably 2.8224MHz.

The digital signals are then modified in a processor such as an equalizer 10

which is able to modify over the whole frequency range not just in the conventional audio band.

The processor 10 may be for example:

an equalizer;

a digital signal mixer;

a processor which encodes audio signals for storage;

a processor which encodes audio signals for transmission; and/or

a processor which encodes audio signals for recording on a medium such as a CD.

The processor would be an n-bit processor if n-bit signals are produced by the converter 8.

Preferably the converter 8 is a 1-bit converter and the processor 10 is a 1-bit processor. An example of a processor is a signal mixer. In the case of a signal mixer the mixer has a plurality of inputs each of which receives an audio signal having components in the range DC to greater than 24kHz as described above.

An example of a 1-bit audio signal mixer is shown in Figure 2 and is described in more detail in co-pending UK patent application 9624671.5 (I-96-24, S96P5063GB00, P/1509) incorporated herein by reference.

Referring to Figure 2, the signal combiner comprises an nth order Delta-Sigma Modulator (DSM) where n is 1 or more. The example shown in a third order DSM (n=3) but n may be greater than 3.

The order of the DSM is defined by the number of integrator sections. In the DSM of Figure 2, there are two inputs 4A and 4B for receiving first and second 1-it input signals. The DSM has: n integrator stages comprising a first stage and n-1 intermediate stages; and a final stage. The first stage comprises a three input adder 61, a first 1-bit multiplier a_1 connected to the first input 4A of the DSM a second 1-bit multiplier b_1 connected to the second input 4B of the DSM, a third 1-bit multiplier connected to the output of the DSM, and an integrator 71. The first, second and third multipliers a_1, b_1, c_1, multiply a 1-bit signal by coefficients A1, B1 and C1 respectively. Each intermediate stage comprises: an adder 62, 63 having four inputs; an integrator 72, 73; a first coefficient multiplier a_2, a_3 connected to the first input of the DSM for multiplying the first 1-bit signal by a coefficient A1, A2, A3; a second

coefficient multiplier b_2,b_3 connected to a second input of the DSM for multiplying the second 1-bit signal by a coefficient B1, B2, B3; and a third coefficient multiplier c_2, c_3 connected to a the output of the DSM for multiplying the 1-bit output signal of the DSM by a third coefficient C2, C3. The adder of each stage adds the output of the integrator of the preceding stage to the output of each 1-bit multiplier connected thereto.

The final stage of the DSM comprises an adder 64 having three inputs; a first coefficient multiplier a_4 for multiplying the first signal by a first coefficient A4; a second coefficient multiplier b4 for multiplying the second signal by a second coefficient B4. The adder 64 adds the output of the integrator 73 of the preceding stage to the outputs of the multipliers a4 and b4. The adder 64 has an output connected to a quantizer Q.

The multipliers a_1 to a_4, b_1 to b_4 and c_1 to c_4 are all 1-bit multipliers, which multiply each bit of the 1-bit signals applied to them by p bit coefficients to produce p bit multiplicands.

The adders 61 to 64 and the integrators 71 to 73 operate on the p bit signals.

The p bit signals are represented in twos complement form for example whereby positive and negative numbers are represented.

The quantizer Q is a comparator having a threshold level of zero. Negative inputs to the quantizer are encoded as -1 (logic 0) and positive inputs as +1 (logical 1), to produce the 1-bit output at output 5.

The first and second 1-bit signals are applied to inputs 4A and 4B. A synchronisation circuit 40 is provided to synchronise the first and second signals to a local clock provided by a clock circuit 41. The synchronisation circuit may separately synchronize the two input signals to the local clock. Clock circuit 41 also controls the clocking of the DSM.

The coefficients A1 to A4, B1 to B4 and C1 to C3 may be chosen using the method described in Annex A to provide

a) circuit stability; and

b) noise shaping.

The coefficients C1 to C3 have fixed values to provide the noise shaping.

The coefficient A1 to A6 and B1 to B4 define zeros of the transfer function

of the input signals and thus control the gain applied to the signals.

In accordance with one embodiment of the present invention, the coefficients A1 to A4 and B1 to B4 are chosen to sum the first and signals in fixed proportions defined by the coefficients. Thus coefficients A1 to A4 may be different from B1 to B4. The coefficients A1 to A4 may equal corresponding coefficients B1 to B4.

In accordance with another embodiment of the present invention, the coefficients A1 to A4 and B1 to B4 are variable to allow the first and second signals to be mixed in variable proportions. The variable coefficients A1 to A4, B1 to B4 are generated by a coefficient generator 42. Generator 42 may be a coefficient store, storing sets of coefficients which are addressed by a variable addressing arrangement responsive to a control signal CS.

Alternatively the coefficients generator 42 maybe a micro computer which generates the coefficients in response to a control signal.

Figure 3 shows, schematically, an example of an integrator 71,72,73. It comprises an adder 30 and a 1-bit delay 31 with a feedback path from the output of the delay to an input of the adder. Thus the output of the delay is added to the signal input to the adder. The adder 30 may be separate from, or implemented by, the adder 61,62,63.

In a modification of the DSM of Figure 3, the second input 4B and the coefficient multipliers B1,B2, B3, B4 are omitted.

The coefficients A1 to A4 (and B1 to B4 if provided) may be chosen to apply a predetermined filter characteristic to the signal in addition to noise shaping.

The microphone 4 of Figure 1 has a bandwidth which is at least DC to greater than 24kHz.

The microphone 4 may be replaced by another audio signal source able to produce signal components in the bandwidth of at least DC to greater than 24kHz. The source may be an audio recorder/reproducer.

Although illustrative embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications can be effected therein by one skilled in the art without departing from the scope and spirit of the invention as defined by the appended claims.